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Single Event Effect in Nano FinFET

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Abstract: FinFET presents more advantages than current bulk CMOS technologies, such as high speed, high density, lower power, more functionality and high scalability. A 3D single event effect model of nano-scale FinFET is simulated by using ISE TCAD. The considered physical models include mobility model, quantum effect model, recombination model and radiation effect model. The effects of the doping concentration, gate voltage, ion energy, parasitic capacitor, and technologies nodes on single event transient current in FinFET are analyzed. The possible mechanisms behind these effects are also presented. The results indicate some potential hardened technologies. It includes decreasing source doping concentration, increasing drain and substrate doping concentration, reducing ion energy, upgrading gate voltage (V_g) and optimizing parasitic capacitor.

Key words: FinFET; single event effect; simulation; harden technology

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1 Introduction

As continued dimensional and functional scaling of CMOS, which eventually will approach fundamental limits, many new alternative devices and microarchitectures for existing or new structures are being explored to maintain the integrated circuits shrinking trends cadence and reduction of cost/function into future decades[1]. Non-planar and multi-gate devices, such as FinFET (Fin field effect transistor)[2−4] and gate-all-around (GAA) FET[5−6] allow better channel control due to their multi-gate structures[1, 4]. FinFET is considered as one of the most promising candidates to replace current bulk CMOS technologies for its high speed, high density, lower power, more functionality and high scalability[1, 3]. For some space and military applications, FinFETs suffer from serious radiation environment, which may cause single event effects(SEEs). In order to achieve a better understanding of SEE on FinFETs, 3D device simulation tools have been explored to perform the radiation effect model, which can accurately simulate SEE in nonplanar nanoscale devices [2, 4, 7−13]. Munteanu *et al.*[6−7] investigated the influence of quantum confinement effects on single event transient (SET) of 32 nm multi-gate nanowire MOSFETs by using 3D quantum numerical simulation. Rathod *et al.*[3] studied the effect of gamma radiation on device characteristics of 25-nm n-channel Ω-FinFET, such as threshold voltage, transfer characteristics, drive current, and so on. Turowski *et al.*[2] presented a physics-based 3D device model of FinFET coupled in mixed-mode with external load circuit and parasitic. Qin *et al.*[4] studied the temperature and drain bias dependency of SET in 25-nm FinFET. The previous works have investigated the effects of ion position[14], technology node scaling[15], ion en-

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ergy and species[16], angle of ion incidence[17] , environmental temperature[4, 8, 17], couple effect[18−19], and drain bias[4] on SEEs. For FinFET technology, the impact of quantum effect[6−7], temperature and power supply voltage[4] on SET is just analyzed. However, the other effects, such as parasitic capacitor, doping concentration, and so on, are also need to study for SET of FinFET.

In order to better understand the mechanism of SEE on nano-scale FinFET, a 3D model of FinFET under SEE is simulated by using Integrated Systems Engineering Technology Computer Aided Design (ISE TCAD) DEVISE simulator[20]. The effects of gate voltage, technology node scaling, parasitic capacitor, doping concentration and ion energy on single event transient drain current of nano FinFET are investigated in this paper. The paper is organized as follows: Section 2 describes the simulation model and theory of FinFET. Section 3 performs the simulation and analysis of transient drain current. Section 4 concludes the paper.

2 Model descriptions

Synopsys sentaurus ISE TCAD is employed to set up the radiation model of 3D nano FinFET. The used simulation tools[20] include DEVISE, MESH, DESSIS, and INSPECT editors. DEVISE has three operational modes: 2D, 3D structure editings, and 3D process emulation. By editing DEVISE, the geometric model, doping and refinement, and submesh of 3D FinFET are achieved. MESH generates meshes of the device by incorporating several different meshing engines, using different meshing techniques and algorithms. It is a dimension-independent tool. The generated meshes are suitable for semiconductor device simulation. DESSIS is a multidimensional, electrothermal, mixed-mode device and circuit simulator for 1D, 2D, and 3D semiconductor devices. It provides physical models, solver methods and radiation effect model for simulating SEEs in semiconductor devices. INSPECT displays the curve and enables users to analyze the data by using both a graphical user interface (GUI) and a script language. Fig. 1 shows the 2D and meshed 3D structures of the modeled n-type FinFET device. The parameters are set as follows. The technology node is 90 nm. The length and the width of the channel are 90, 60 nm, respectively. The size of source/drain (silicon) region is 70 nm×70 nm×40 nm. The size of box (oxide) is 180 nm×90 nm×40 nm. The thickness of gate oxide is 2 nm. The constant doping concentrations of source and drain are 5×10^{19}, 1×10^{20} Arsenic Active Concentration, respectively. The constant doping of substract is 1×10^{16} Boron Active Concentration. The drain supply voltage is set to 2 V. The possible physical models are doping dependent mobility degradation model, Philips unified mobility model, high field saturation model, band gap and electron affinity model, hydrodynamic model, Shockley-Read-Hall (SRH) and Auger recombination models, Fermi statistics model, and heavy ion model. The position of heavy ion incidence is the drain region of FinFET and the incidence time is 5 ps. The run time is set to 1 ns.

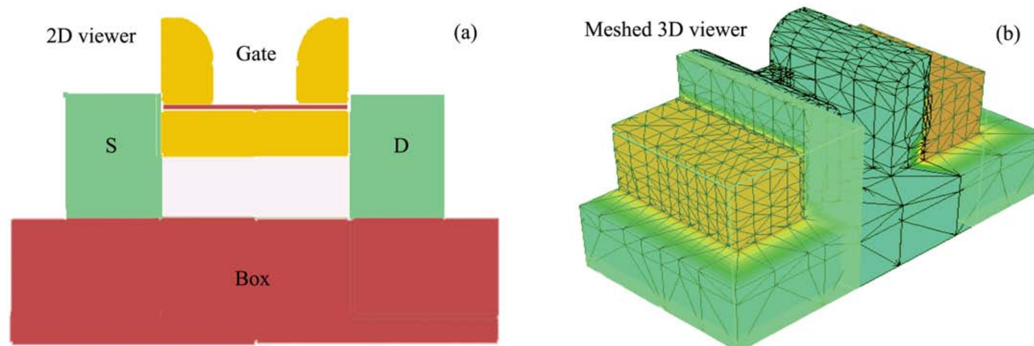

Fig. 1 (color online) Structures of FinFET device.

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3 Simulation results and analysis

By using ISE TCAD tools, the simulation for SEE in the modeled FinFET is performed. The impacts of the doping concentration, gate voltage, ions energy, parasitic capacitor, and technology nodes on SEE in FinFET are analyzed.

3.1 Effect of doping concentration

When ions strike into the semiconductor devices, silicon material through which the ions pass is ionized, leaving behind lots of electron-hole pairs. The doping carriers of the electrodes of FinFET will neutralize a number of the ionized electron-hole pairs. Linear energy transfer (LET) of ions is set to 0.5 pC/μm (For source doping analysis, LET is 0.1 pC/μm.). The voltage of the gate is set to 0.1 V. Figs. 2～4 show the simulation results.

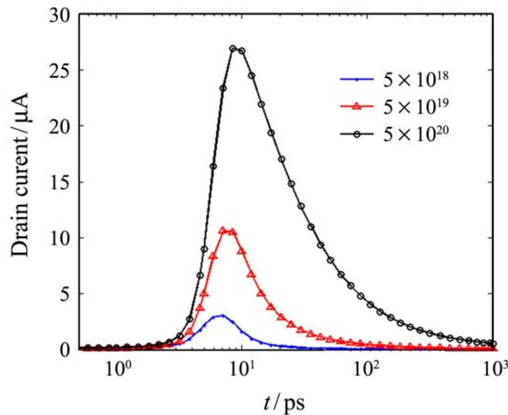

Fig. 2 (color online) Effect of source doping concentration on SET.

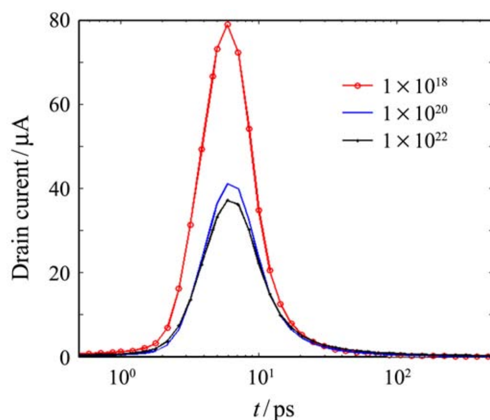

Fig. 3 (color online) Effect of drain doping concentration on SET.

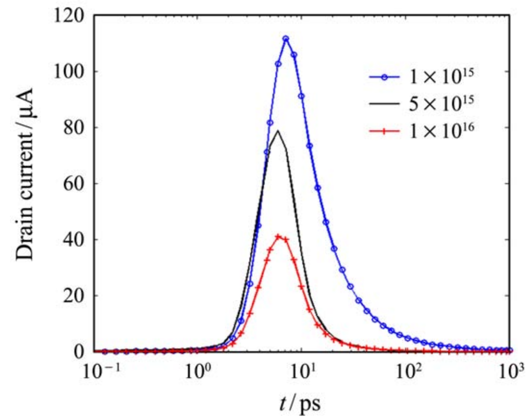

Fig. 4 (color online) Effect of substrate doping concentration on SET.

In Fig. 2, as the source doping concentration increasing, the amplitude and width of the SET current pulse is dramatically enhanced. The max SET current value is 10.6 μA at 5×10^{19} source doping concentration, while the value is 27 μA at 5×10^{20} doping concentration. The widths of current pulse at 5×10^{19} and 5×10^{20} doping concentrations are 9, 56 ps, respectively. It can be concluded that the source doping concentration increase will deteriorate the effect of SEE in FinFET. It may be due to that the carriers of generated current come from the source electrode. Therefore, when the source doping concentration is increased where the carriers is larger, the source electrode will provide more carriers to generate larger current.

In Fig. 3, instead of the effect of the source doping on SET, the SET drain current decreases when the drain doping concentration increases. However, the decrease of the current pulse width is not obvious as the drain doping concentration increasing. The reason is that the carriers of the drain electrode can neutralize a number of the ionized electron-hole pairs. So the increase of the drain carrier concentration will improve the immunity to SEE. However, when the drain doping concentration (such as 1×10^{22}) is larger than 1×10^{20}, the immunity to SET is hardly improved.

In Fig. 4, like as the trend of the effect of the drain doping on SET, the drain current pulse becomes weak as the substrate doping concentration increasing. The decrease of the drain current due to

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the substrate doping concentration increase is more than one due to the source doping. The max current value increases three times with the substrate doping concentration decreasing one magnitude (from 1×10^{16} to 1×10^{15}) due to that the carriers of the substrate could neutralize the ionized electron-hole pairs when the ions strike into the device. Hence, the hardened technology by increasing the substrate doping concentration is more attractive than other process technologies.

3.2 Effect of gate voltage

The gate voltage (V_g) controls the transport of the carriers from the source electrode to the drain one. The transport of the ionized electron-hole pairs due to SEE are importantly influenced by the gate voltage. The simulation is performed with the range of the gate voltage from 0.1 to 2 V. Fig. 5 shows the SET currents for different gate voltages.

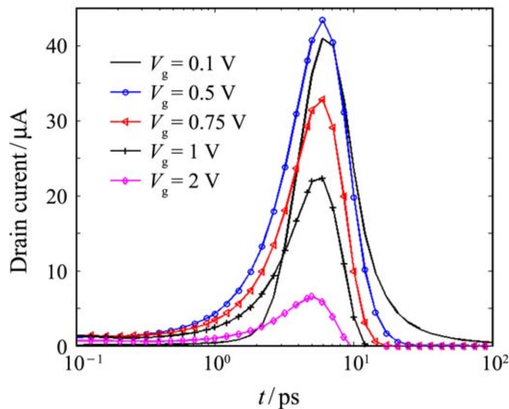

Fig. 5 (color online) Effect of gate voltage on SET.

When the ions strike into MOSFET, the drain of an n-type MOSFET that is initially at a high voltage (V_{DD} or "1") will see a negative voltage spike while a p-type MOSFET drain that is initially at ground ("0") will experience a positive voltage spike[11−12]. In Fig. 5, the SET drain current decreases as the gate voltage increasing from 0.1 to 2 V. As well-known, the sensitive sites of SEE are the surroundings of the reverse-biased drain junctions of the transistor biased in the off state. The modeled FinFET is an n-type FET. When the gate voltage is set at a low voltage (such as 0.1 V), the state of FET is in the off. FET is more sensitive to SEE. It means that the higher the gate voltage of n-type FinFET is, the weaker the SET drain current will be, although the static drain current is high at a high gate voltage.

3.3 Effect of ions energy

The SET current pulse depends on LET of the incidence ions which is determined by the ions energy[16]. The effect of LET on the SET current in FinFET is analyzed with the range from 0.01 to 1 pC/μm. The results are shown in Fig. 6.

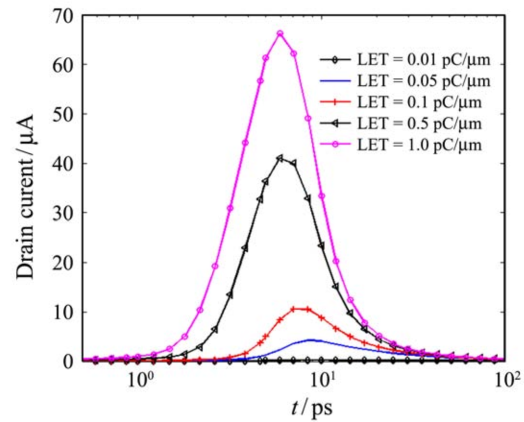

Fig. 6 (color online) Effect of LET on SET.

In Fig. 6, the SET drain current becomes stronger with the increase of LET. Both of the amplitude and width of the SET pulse enhances as the LET increasing. The max drain current values increases from 0.2 to 66.3 μA as LET changing from 0.01 to 1 pC/μm. The larger LET is, the more energy is transferred to the material where the more electron-hole pairs will be ionized.

3.4 Effect of parasitic capacitor

As the transistors size scaling down, the influence of the parasitic capacitor on the electrical properties of FET is more and more prominent. For SEE, the parasitic capacitor will charge and discharge when the ions strikes into the drain of FET. The LET is set as 0.5 pC/μm and the gate voltage is 0.1 V. The simulation results are shown in Figs. 7 and 8.

Fig. 7 shows the drain current pulse with different capacitors, while the max pulse values are shown in Fig. 8. From the results, it can be found that as the capacitor changing from 0.05 to 5 fF, the corresponding to the drain current pulse can be approxi-

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mately divide into two cases. One case is the pulse when the capacitor is 0.5 fF and the other case is the pulses with other capacitors values. From Fig. 8, it can be concluded that the max current value corresponding to 0.5 fF is less than the values with other capacitors. Therefore, in order to improve the immunity to SET, the capacitor of FinFET may be optimized to a fine value (such as 0.5 fF). If the best optimized value found, the immunity to SET in FinFET will be greatly improved (In this case, the current pulse in the other capacitor value is three times than one in the best value 0.5 fF).

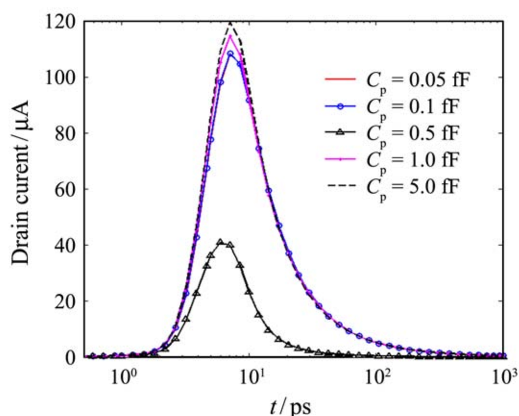

Fig. 7 (color online) Effect of parasitic capacitor on SET.

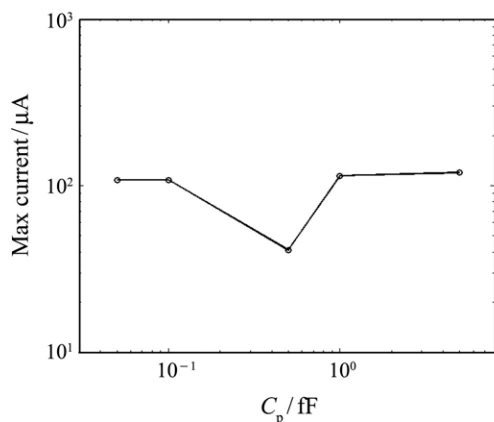

Fig. 8 Max SET currents for different parasitic capacitors.

3.5 Effect of transistor size scaling

With the technologies nodes reducing, the gate length of the transistor is scaling down. The less the transistor size is, the more immune to SEE it is. We analyze the technologies nodes of 45, 65, 90 nm. The results are shown in Fig. 9.

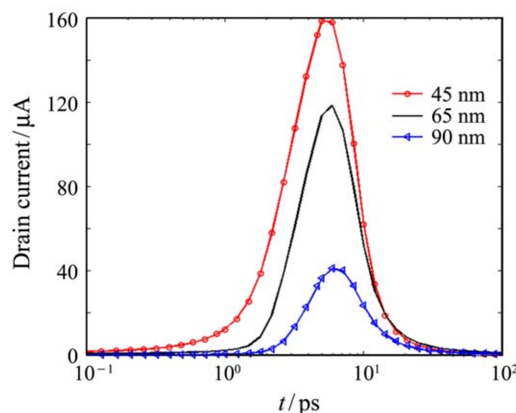

Fig. 9 (color online) Effect of technology nodes scaling on SET.

In Fig. 9, the pulse widths of 45, 65, 90 nm are 10.5, 9.3, and 8.1 ps, respectively. The max current values for 45, 65, 90 nm, are 159, 118 and 41 μA, respectively. It indicates that the sensitivity to SEE greatly increases with the gate length reducing from 90 to 45 nm. Therefore, a hardened technology is realized by adjusting to the transistors sizes, especially the more sensitive FET to SEE.

4 Conclusions

Due to its high speed, high density, lower power, and high scalability, FinFET is considered as one of the most promising candidates to replace CMOS technologies. For better understanding the mechanism of SEE in FinFET, a 3D simulation model of nano-scale FinFET is built by ISE TCAD. The used physical models consider many basic mechanisms, such as quantum effect, Fermi statistic, and so on. The effects of doping concentration, gate voltage, LET, parasitic capacitor and technologies nodes on SET current pulse in FinFET are modeled. Some mechanisms behind these trends are analyzed. Based on these simulation results, a few potential hardened technologies are proposed, such as adjusting to the doping concentration, optimized the parasitic capacitor, etc.

References:

[1] Semiconductor Industry Association. International technology roadmap for semiconductors [EB/OL]. [2011-01-12]. http://public.itrs.net.

http://www.npr.ac.cn

[2] TUROWSKI M, RAMAN A, XIONG W. Physics-based modeling of nonplanar nanodevices (FinFETs) and their response to radiation[C]//18th International conference on Mixed Design of Integrated Circuits and Systems. Gliwice, Poland, 2011: 460.

[3] RATHOD SS, SAXENA AK, DASGUPTA S. Microelectronics Journal, 2011, **42**: 165.

[4] QIN J, CHEN S, LI D, *et al.* Chinese Physics B, 2012, **21**(8): 089401.

[5] KAUSHAL G, RATHOD SS, MAHESHWARAM S, *et al.* IEEE Transactions on Electron Devices, 2012, **59**(5): 1563.

[6] MUNTEANU D, AUTRAN JL, FERLET-CAVROIS V, *et al.* IEEE Transactions on Nuclear Science, 2007, **54**(4): 994.

[7] MUNTEANU D, FERLET-CAVROIS V, AUTRAN JL, *et al.* IEEE Transactions on Nuclear Science, 2006, **53**(6): 3363.

[8] ALVARADO J, BOUFOUSS E, KILCHYTSKA V, *et al.* Microelectronics Reliability, 2010, **50**: 1852.

[9] CHATTERJEE I, NARASIMHAM B, MAHATME NN, *et al.* IEEE Transactions on Nuclear Science, 2011, **58**(6): 2761.

[10] MOEN K A, NAJAFIZADEH L, SEUNGWOO J, *et al.* IEEE Transactions on Nuclear Science, 2011, **58**(3): 877.

[11] DODD PE, MASSENGILL LW. IEEE Transactions on Nuclear Science, 2003, **50**(3): 583.

[12] MUNTEANU D, JL AUTRAN. IEEE Transactions on Nuclear Science, 2008, **55**(4): 1854.

[13] LAIRD JS, HIRAO T, ONODA S, *et al.* Nuclear Instruments and Methods in Physics Research B, 2003, **206**: 36.

[14] HIRAO T, NASHIYAMA I, KAMIYA T, *et al.* Nuclear Instruments and Methods in Physics Research B, 1997, **130**: 486.

[15] BENEDETTO JM, EATON PH, MAVIS DG, *et al.* IEEE Transactions on Nuclear Science, 2006, **53**(6): 3462.

[16] REED RA, WELLER RA, MENDENHALL MH, *et al.* IEEE Transactions on Nuclear Science, 2007, **54**(6): 2312.

[17] HUTSON JM, PELLISH JD, BOSELLI G, *et al.* IEEE Transactions on Nuclear Science, 2007, **54**(6): 2541.

[18] LIU BJ, CAI L, YANG XK, *et al.* Microelectronics Journal, 2012, **43**(1): 63.

[19] LIU BJ, CAI L, ZHU J. IEEE Transactions on Nuclear Science, 2012, **59**(4): 1621.

[20] Synopsys Sentaurus TCAD Tools[EB/OL]. [2004-01-01]. http://www.synopsys.com/products/tcad/tcad.html.

纳米 FinFET 器件的单粒子效应研究

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摘要： FinFET 器件比主流 CMOS 技术表现出更多优势，如快速、高集成度、低功耗、多功能性和强扩展性，基于 ISE TCAD，考虑迁移率、量子效应、载流子重组、辐射效应等的影响，建立了一种纳米 FinFET 器件 SEE 的 3D 仿真模型。分析了工艺掺杂浓度、栅压、粒子能量、寄生电容及技术节点等对单粒子瞬态电流的影响，并探讨了其影响机制。基于此分析，找到了一些潜在的工艺加固技术，如降低源极掺杂浓度、增加漏极和衬底的掺杂浓度、减少粒子能量、降低栅压、优化寄生电容等。

关键词： FinFET; 单粒子效应; 仿真; 加固技术

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