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Design and Simulation of Track/Hold Circuit with CMOS FET for Particle Detector*

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Abstract: In this paper, the objective is to realize a Track/Hold Circuit for silicon strip, Si(Li), CdZnTe and CsI detectors etc. By using CMOS transistor to implement various components in electronic circuit, the Track and Hold circuit only made with CMOS FET is succeeded to be designed and simulated. Performance was characterized using PSPICE simulator with BSIMV3.3 parameters of the Proteus. Several measurements of acquisition time can be made from 60 ns to 4.44 μs related to the output resistance, and the integral nonlinearity is good.

Key words: Track/Hold; CMOS transistor; peak value; simulation

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1 Introduction

In nuclear and particle physics, the energy of particles is often measured by means of semiconductor detectors. The sensors produce a current pulse with a total amount of charge proportional to the absorbed energy. This charge is then integrated in a charge sensitive amplifier, resulting in a voltage step. To increase the signal-to-noise ratio, the step signal is usually filtered by a pulse shaping amplifier(PSA). The resulting output signal is a voltage pulse with a peaking time typically between 1 to several ps. The amplitude value of the output signal of the PSA contains the information about the energy of the particle. To digitize the amplitude value, for processing reasons, the amplitude value should be sampled and held by a Track/Hold circuit.

The Track/Hold function is to sample the input signal at a precise instant and hold the value of the sample constant during the analog-to-digital conversion process. The most basic Track/Hold circuit only consists of a switch and a capacitor[1]. If the switch and the capacitor are assumed to be ideal, i.e. they do not consume any power due to parasitic and other non ideal effects, the minimum theoretical power consumption can be calculated when performing Track/Hold. The worst case occurs when the maximal input voltage is sampled on the capacitor every period[2]. In this research, front-end circuit is designed to grab an interesting signal. This is often accomplished with a circuit that tracks or follows the input signal, until an interesting signal is detected, and at this point the circuit holds the resulting analog level for a long enough time that the analog signal can be converted to a digital value and stored. Such a circuit is called a Track/Hold circuit. The key element that

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actually stores the analog signal is a capacitor. The design of the capacitors is crucial for the performance of the overall Track/Hold circuit[3]. A poorly designed capacitor can degrade the performance by for example introducing harmonics and some other unideal behaviour. The purpose with this project is to design a front-end Track/Hold, to be used together with an A/D converter. It is to be designed in CMOS process, which only allows a supply voltage of ±2 V. The main design consideration is to minimize the power consumption, since the circuit is supposed also to be used in a mobile transceiver.

2 Track/Hold Principle

The Track/Hold consists of some sort of sampling switch, a sampling capacitor and a buffer, shown in Fig. 1. It functions by sampling the input signal at a precise instant and hold the value of the sample constant during the analog-to-digital conversion process. The design, Fig. 2 below, is composed by the source follower PMOS, followed by a CMOS transistor played the role of switch, two CMOS transistors in parallel one implemented as capacitor and the another implemented as a switch, a source follower NMOS at the end. We choose PMOS follower in the input and NMOS in the output to compensate the DC level. The simulation gives the result found in the Fig. 3(a) according to the specifications of Track/Hold. We need to keep the level of sample constant as long as possible for acquisition. To hold the sample constant shown in Fig. 3(b), the output resistor of the first follower should be controlled (the control system stands as a parallel resistance with the output resistance of the first follower to change DC level during Hold time). To realize this success shown in Fig. 3(b), the improvement of Fig. 2 gives the result shown in Fig. 4, where CMOS M23 stands as the parallel resistance with output resistance of the first follower to bring up DC level so that CMOS M8 look like a switch OFF element (big equivalent resistance) which will not allow, during the Hold phase, transistor CMOS M22 implemented as capacitor to be discharged. The transistor CMOS M23 is controlled by Track/Hold signal through CMOS M25 transistor.

The main design parameters are given in Table 1.

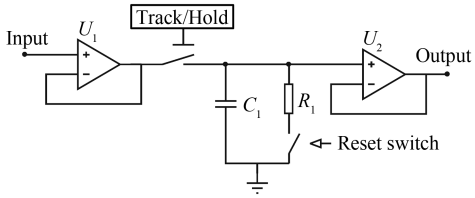

Fig. 1 Block diagram of Track/Hold circuit principle.

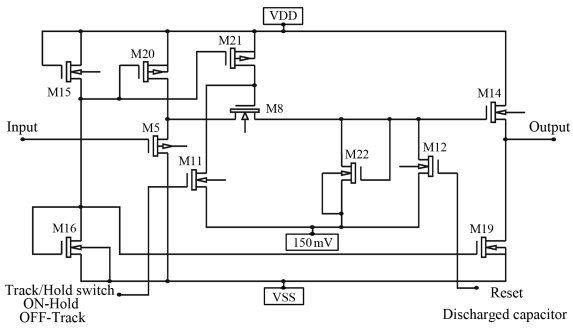

Fig. 2 Track/Hold circuit with low quality result.

Table 1 The design parameters of Track/Hold peak detector

Parameters	Values
Power supplies	$VDD=+2$ V, $VSS=-2$ V
Transistor M5 parameter	$K=80\times10^{-1}$ A/V^2, $VT=-0.1$ V
Transistor M8 parameter	$K=2\times10^{-3}$ A/V^2, $VT=+0.5$ V
Transistor M11 parameter	$K=2\times10^{-3}$ A/V^2, $VT=+0.5$ V
Transistor M14 parameter	$K=80\times10^{-1}$ A/V^2, $VT=+0.1$ V
Transistor M15 parameter	$K=4\times10^{-2}$ A/V^2, $VT=-1$ V
Transistor M19 parameter	$K=4\times10^{-2}$ A/V^2, $VT=+1$ V
Transistor M20 parameter	$K=4\times10^{-2}$ A/V^2, $VT=-1$ V
Transistor M21 parameter	$K=4\times10^{-5}$ A/V^2, $VT=-1$ V
Transistor M23 parameter	$K=30\times10^{-2}$ A/V^2, $VT=-1$ V
Transistor M24 parameter	$K=4\times10^{-5}$ A/V^2, $VT=-1$ V
Transistor M25 parameter	$K=2\times10^{-3}$ A/V^2, $VT=+0.5$ V
Input amplitude range	50 mV to 2 V
Output resistance	25 Ω
Bias Transistors M11, M12, M22, M25	+150 mV
Storage capacitor C1	1 nF to 10 pF

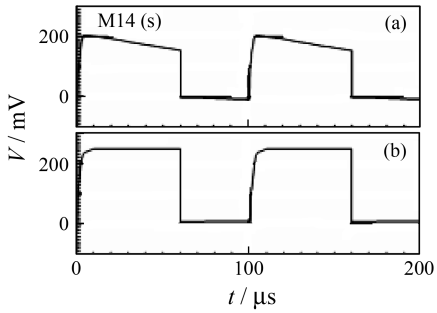

Fig. 3　(a) Output signal from low quality circuit, (b) Output signal from good quality circuit.

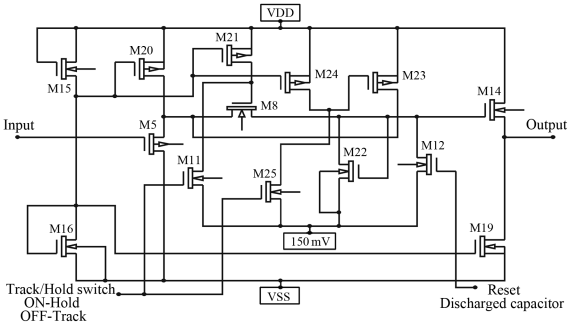

Fig. 4　Track/Hold circuit with good quality result.

3　Achievement

From Fig. 1, we wonder how the small size of capacitor C1 can stand as long as possible to keep constant the peak value permitting to acquisition time exploitation. The Fig. 2 built according to the principle of Track/Hold shows the difficulty to keep the peak value constant during the Hold phase. Investigation has proved that the capacitor will discharge during the Hold phase in one way because after Track, the DC level of output Buffer1 is lower than the level of capacitor C1, then the capacitor has to be discharged through the equivalent resistance of transistor M8 implemented as a switch OFF(equivalent resistance), in another way the input resistor of Buffer 2 and equivalent resistance of transistor M12 implemented as a switch OFF will also discharge the capacitor C1 during the Hold phase. To find the solution we study and analyze how to reduce the impact of these elements during the Track/Hold phase. Step by step we realize it is better to control the output resistance of Buffer 1 to make DC level of the first Buffer output rise up and exceed the level of capacitor C1 after Track phase. The system composed by the transistors M23, M24 and M25 brings the correction expected and Fig. 4 permits to maintain constant the amplitude of signal at the output after Track phase while waiting reset moment to be discharged. For easy didactic exploitation of the circuit, Fig. 4 is simplified as shown in Fig. 5.

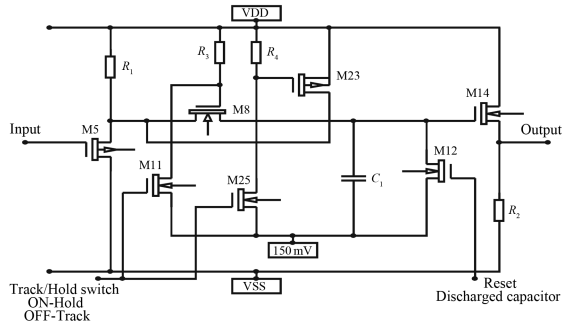

Fig. 5　Schematic drawing of Track/Hold.

4　Simulation Results

Before input signal is sent to circuit for simulation, the DC level of the first buffer output is 141 mV and the output of the second buffer is 0 V. With the signal of 250 mV for peak value, the output is maintaining constant slightly under 250 mV during Hold period, while through the transistors (M23, M24, and M25) controlled by Track/Hold signal, the DC level of the first buffer output changes to 380 mV for avoiding the level of capacitor C1 to be discharged during acquisition time. We should not forget that the output information can be shifted according to DC level when we try to adjust the value around 150 mV DC for Source level of transistors M11, M12 and M25 connected together[4]. Also the value of 150 mV that we choose is to compensate the DC level and to control the peak signal of the particle. Fig. 6 shows the forms of signal at different level when a particle peak value is detected to be analyzed further.

If these results seem to be acceptable, we should not forget the specification of real Track/Hold circuit. Acquisition Time is the time which takes to reacquire the input signal when switching from the Hold to Track mode. This time interval starts at 50% of the clock transition and ends when the input signal is reacquired to within a specified

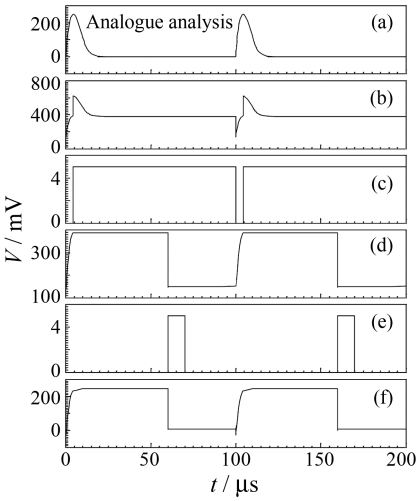

Fig. 6 Forms of signal during detection of particle.
(a) Input signal, (b) Signal immediately after Buffer1, (c) Track/Hold switch instruction, (d) Signal immediately before Buffer 2, (e) Reset instruction, (f) Output signal after Buffer 2.

accuracy at the output. This specification does not include the track-to-hold settling time[5]. According to the specifications defined in the circuit, the acquisition time of 4.44 μs with 25 Ω output resistance is realized. From measurement, if we consider our output before buffer 2, this value is closed to zero at the level of C1. Also if the output resistance increases, the acquisition time will be reduced and which will be 60 ns when the measurement was made at the output of buffer 2[6]. For exploitation of the circuit, the integral nonlinearity has been measured and the results are shown in Fig. 7. The value of integral nonlinearity is 1.7% for input range from 50 mV to 600 mV, and it will be 2.7% for input range from 50 mV to 1300 mV. The main simulated specifications are given in Table 2.

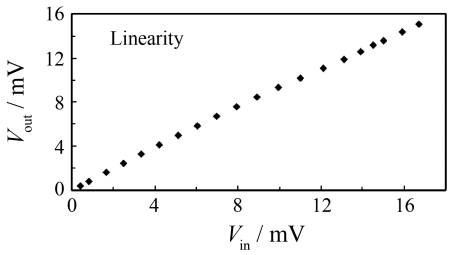

Fig. 7 Measured integral nonlinearity of the Track/Hold.

Table 2 The main simulated specifications

Parameters	Value
Gain	0.95
Integral nonlinearity	1.7%
Switch speed	0.36 ns
Droop rate	661 mV/ns
SNR	60.3 dB
SNDR	33 dB

5 Conclusions

After designing the new peak detector with CMOS FET implemented for each component, computer simulation was carried out by PSPICE simulator using BSIMV3.3 parameters of the Proteus and the results obtained are closer to the specifications of real Track/Hold system. The advantage of this design is benefit to develop CMOS-based Application Specific Integrated Circuit. The acquisition time for this purpose can be less than 4.44 μs and closed to zero if we increase the value of output resistance; the circuit also has good integral nonlinearity. We intend to improve these results in the near future by controlling the parameters of CMOS equivalent circuit when it is used as resistor, capacitor or diode etc.

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用于粒子探测器的 CMOS FET 采样保持电路的设计与仿真*

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摘　要: 介绍了一个峰保持电路。该电路适用于 silicon strip, Si(Li), CdZnTe and CsI 等探测器, 实现采样-保持功能。已成功进行了基于 CMOS FET 的采样-保持电路的设计和仿真, 通过使用 Proteus 的 PSPICE 仿真器和 BSIMV3.3 模型参数完成了电路性能的仿真。同时, 实现了采样时间可在 60 ns 到 4.44 μs 范围内进行选择, 该电路具有较好的线性。

关键词: 采样保持; CMOS 场效应管; 峰值; 仿真

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